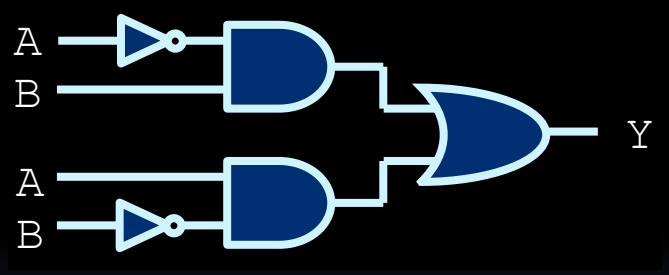
Lecture 2 Review

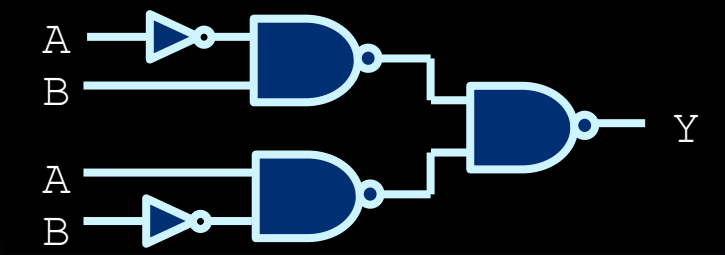
Path Intergrals over Complex Plane

- Let $f(z): \mathbb{C} \to \mathbb{R}$
- $\int_{z_1}^{z_2} f(z)dz = ?$

Lecture 2 Review

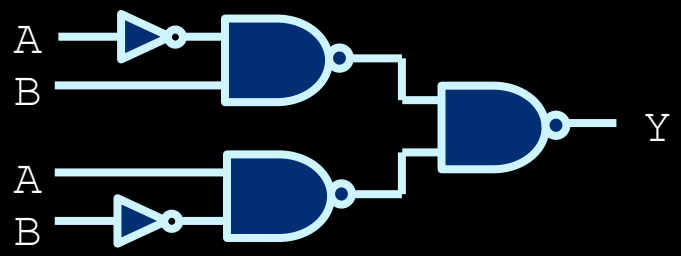
- Question #1:
  - Express XOR using only NAND and NOT gates

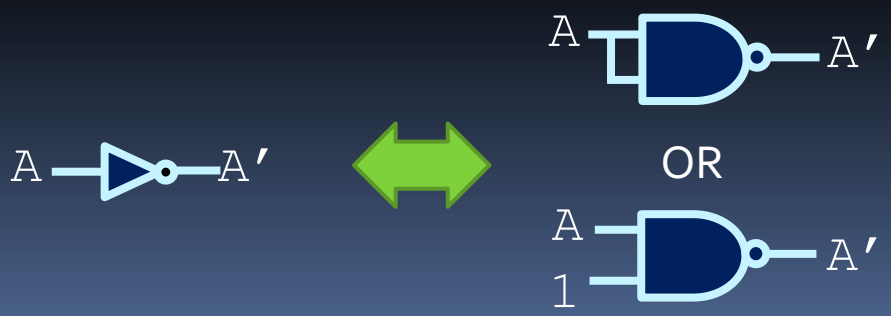




Lecture 2 Review

- Question #1b:
  - Implement XOR using only NAND gates
  - HINT: Implement NOT using NAND gates





Lecture 2 Review

- Question #2a:
  - Construct the truth table for the following requirement

When A is off, I want the output to be high whenever one of B or C are 1, but low when they're both 1 or both 0. When A is on, I want the output to be high when B and C are both 0 or both 1, and low otherwise.

A	B	C	Y
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Lecture 2 Review

- Question #2a:
  - Construct the truth table for the following requirement

When A is off, I want the output to be high whenever one of B or C are 1, but low when they're both 1 or both 0. When A is on, I want the output to be high when B and C are both 0 or both 1, and low otherwise.

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Lecture 2 Review

- Question #2b:
  - What are the minterms for the following table?
  - What is the SOM expression (non reduced)

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

$$Y = m_1 + m_2 + m_4 + m_7$$

$$Y = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$

Lecture 2 Review

- Question #3a
  - Complete the truth table

$$Y = m_0 + m_1 + m_2 + m_5 + m_7 + m_8 + m_9 + m_{10} + m_{13} + m_{15}$$

A	B	C	D	X
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Lecture 2 Review

- Question #3b
  - Construct the K-Map

	$\overline{C} \cdot \overline{D}$	$\overline{C} \cdot D$	$C \cdot D$	$C \cdot \overline{D}$
$\overline{A} \cdot \overline{B}$				
$\overline{A} \cdot B$				
$A \cdot B$				
$A \cdot \overline{B}$				

A	B	C	D	X
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

Lecture 2 Review

- Question #3c:
  - Find the groupings and reduce the expression

	$\overline{C} \cdot \overline{D}$	$\overline{C} \cdot D$	$C \cdot D$	$C \cdot \overline{D}$
$\overline{A} \cdot \overline{B}$	1	1	0	1
$\overline{A} \cdot B$	0	1	1	0
$A \cdot B$	0	1	1	0
$A \cdot \overline{B}$	1	1	0	1

$$Y = BD + \overline{C}D + \overline{B}\overline{D}$$

Lecture 3 review

Question #1

a) How do you write the number 78 as an 8-bit binary number?

b) What is the two's complement of `01101101`?

`10010011`

c) What is `11001010` In decimal?

Unsigned 202

Signed (2's complement) -54

Question #1

d) What is the sum of `01101101` and `01101101`?

`011011010`

Don't forget to add the extra 0 to the front

- Adding a number to itself → multiply by 2
- Multiply by 2 → shift bits to the left

Question #2

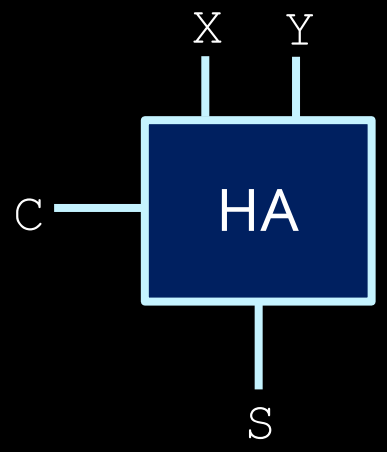
- What groupings are in the K-map on the right?

	$\overline{C} \cdot \overline{D}$	$C \cdot \overline{D}$	$C \cdot D$	$\overline{C} \cdot D$
$\overline{A} \cdot \overline{B}$	1	1	X	1
$A \cdot \overline{B}$	X	0	X	1
$A \cdot B$	1	X	X	1
$\overline{A} \cdot B$	1	X	0	X

- What logic equations do these groupings represent?

$$\overline{A} \cdot \overline{B} + \overline{C}$$

Question #3



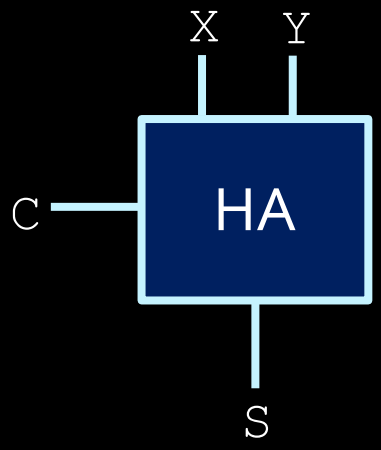
- Implement a half adder in Verilog.
- Step 1: What is the half adder logic equation?

$$C = X \cdot Y \qquad S = X \cdot \overline{Y} + \overline{X} \cdot Y = X \oplus Y$$

- Step 2: Equivalent Verilog components.

```
assign C = X & Y;
assign S = X & ~Y | ~X & Y;
```

Question #3 (cont'd)



- Step 3: What is the complete Verilog code for this device?

```
module half_adder(X, Y, C, S);
    input X, Y;
    output C, S;

    assign C = X & Y;
    assign S = X & ~Y | ~X & Y;
endmodule
```