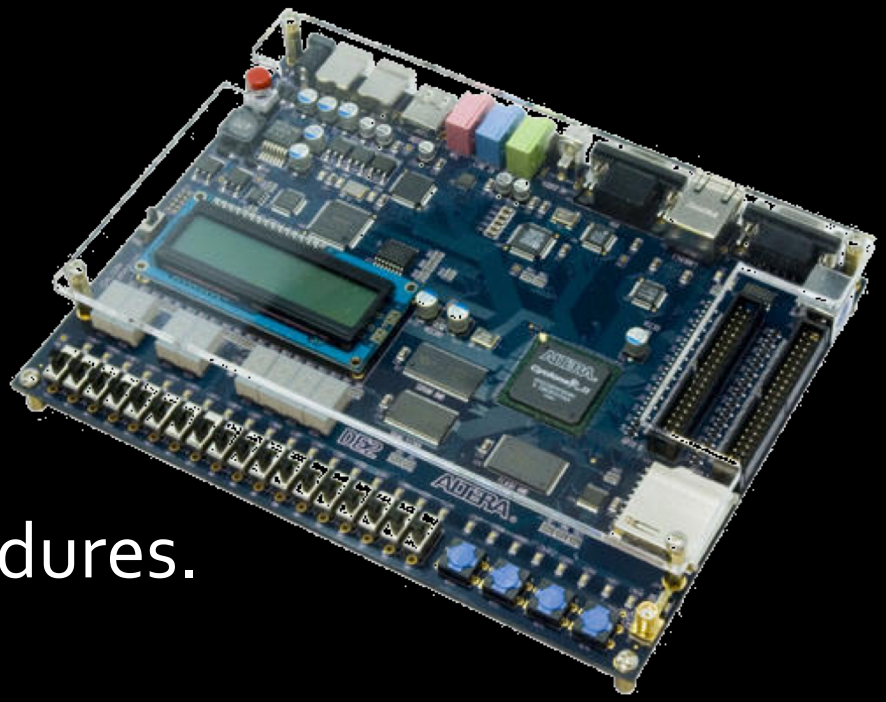
Week 1 Tutorial: Lab Preview & Building Gates

Lab 0

- Using the DE2.
- Creating a project using Quartus II.
- Lab rules and procedures.



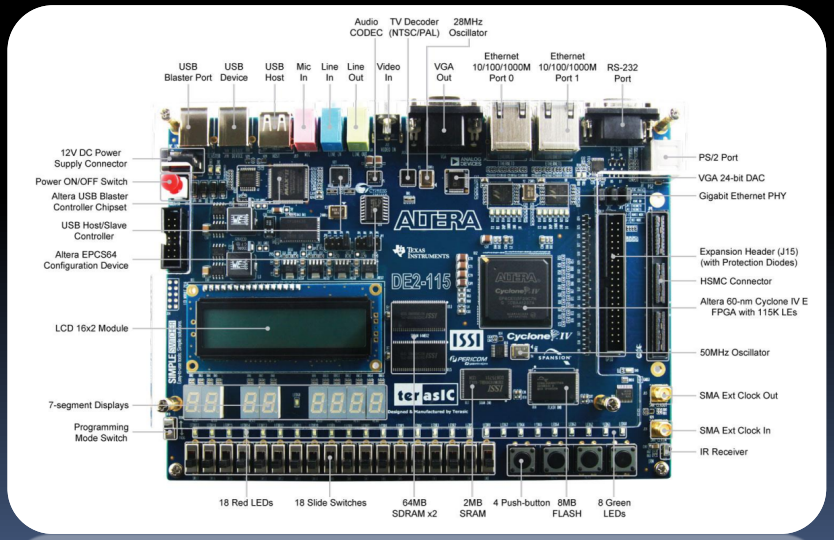
Admin

- Don't forget your pre-lab!
  - Each student brings their own pre-lab printout
- Lab reports/code/whatever due by Friday at the end of each week
- Upload to Quercus
- Each member of the pair must upload or you won't both get the marks
  - Both pairs can upload the same post-lab package.
- Don't forget your pre-lab

What is a DE2?

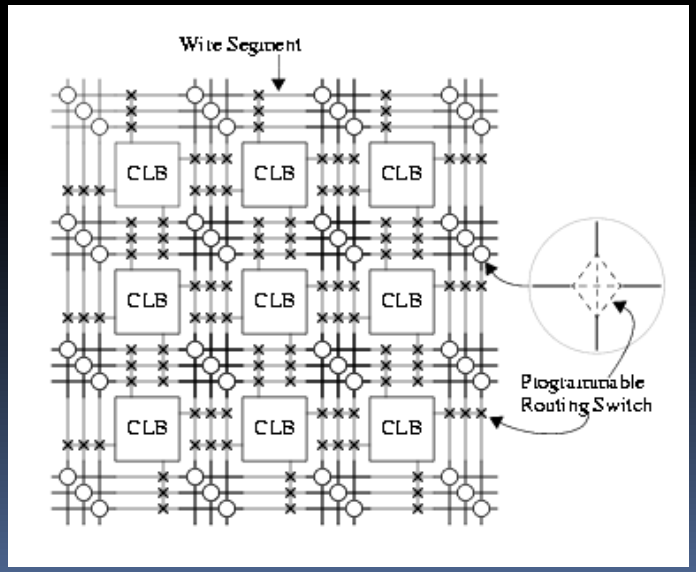
An educational circuit board with:

- Altera Cyclone IV 4CE115 FPGA
- Two 64 MB SDRAM, 2MB SRAM, 8 MB Flash
- Eight 7-segment displays
- SD memory card slot
- 16 x 2 LCD display
- 18 toggle switches
- 18 red LEDs
- 9 green LEDs
- Four debounced pushbutton switches

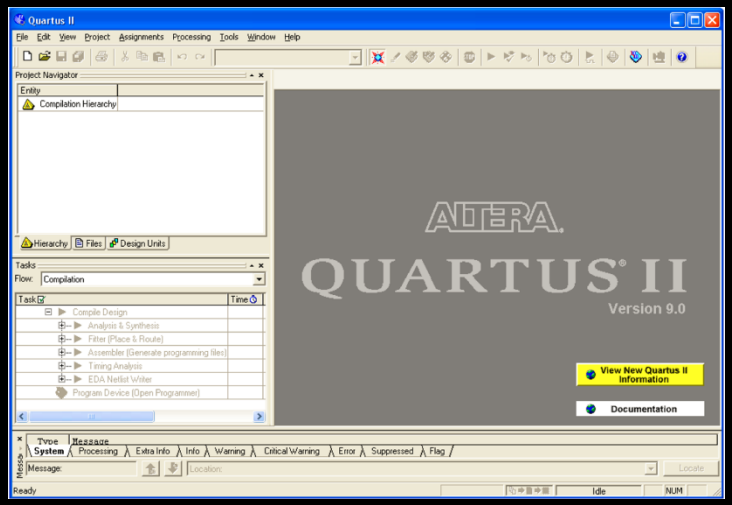


What does that mean?

- Key term: FPGA.
  - Stands for Field Programmable Gate Array.
  - A regular network of logic that can be programmed and reprogrammed to implement any circuit.
  - In Lab 0, we'll be programming gates manually, starting with Lab 1, we'll be using Verilog



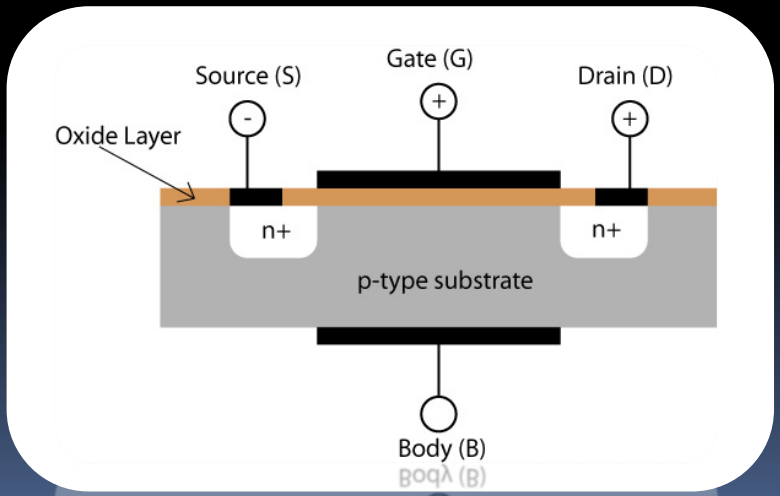
Quartus II



- Tool provided by Altera that compiles Verilog programs, and uploads the result to the FPGA.
- Software built for engineers, not for the general public (not the most user friendly)

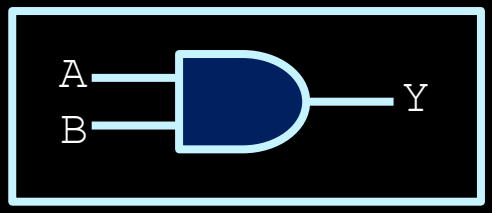
Week 1 Review

- Basic gates
- Properties of electricity
- Semiconductors,
  - Doping (n-type and p-type)
- p-n junctions
- Transistors
  - MOSFETs
- Building gates

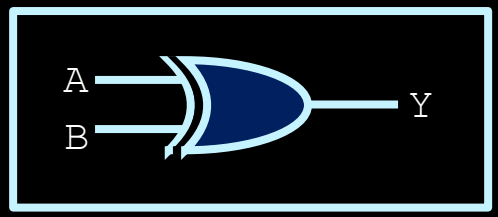


Question 1

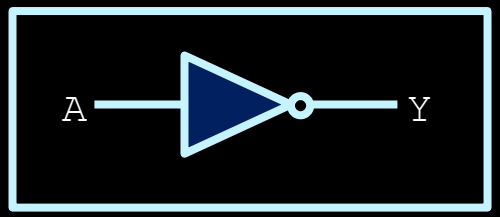
- What are the names and truth table values for the following gates?



A	B	Y
0	0	
0	1	
1	0	
1	1	



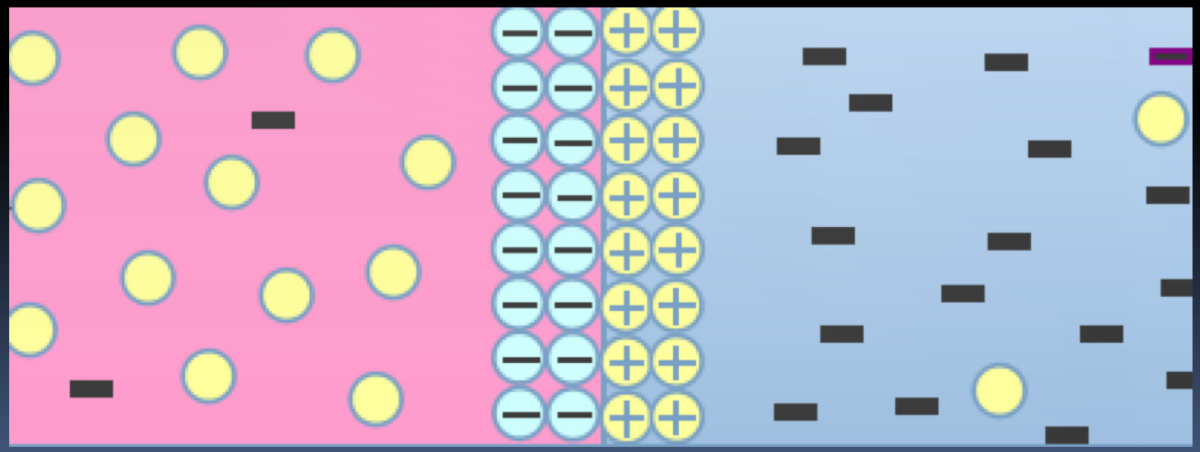
A	B	Y
0	0	
0	1	
1	0	
1	1	



A	Y
0	
1	

Question 2

- Which areas of the PN junction below are positively/negatively/neutrally charged?
- What would happen if we added a negative charge (source of electrons) to the left side of the junction?



Transistor review

- Logic gates are built from transistors

This transistor is called nMOS

It conducts (i.e., acts as a closed switch) if we apply 5 Volts (logic-1) at its gate.

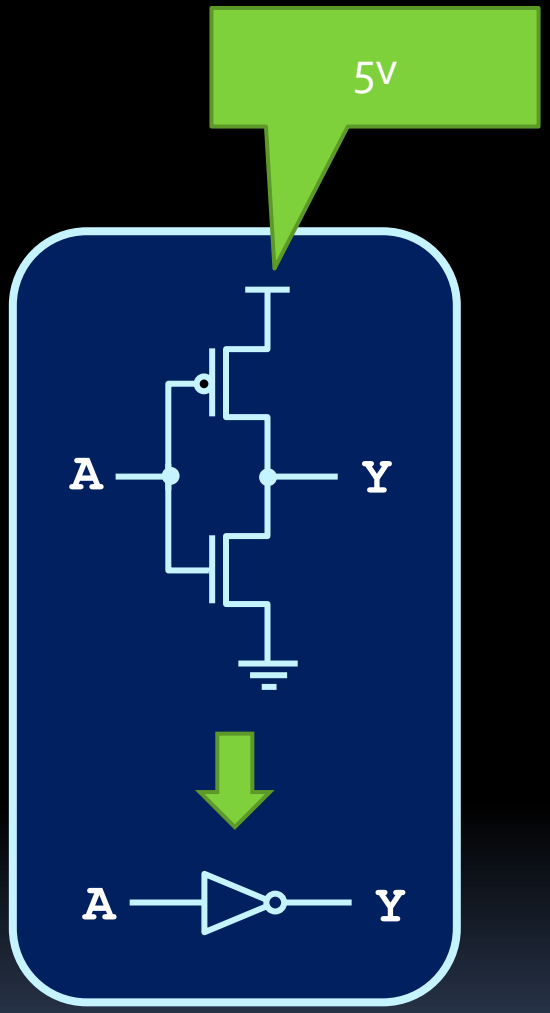
This transistor is called pMOS

It conducts (i.e., acts as a closed switch, if we apply 0 Volts (logic-0 , Gnd) at its gate.

NOT gate

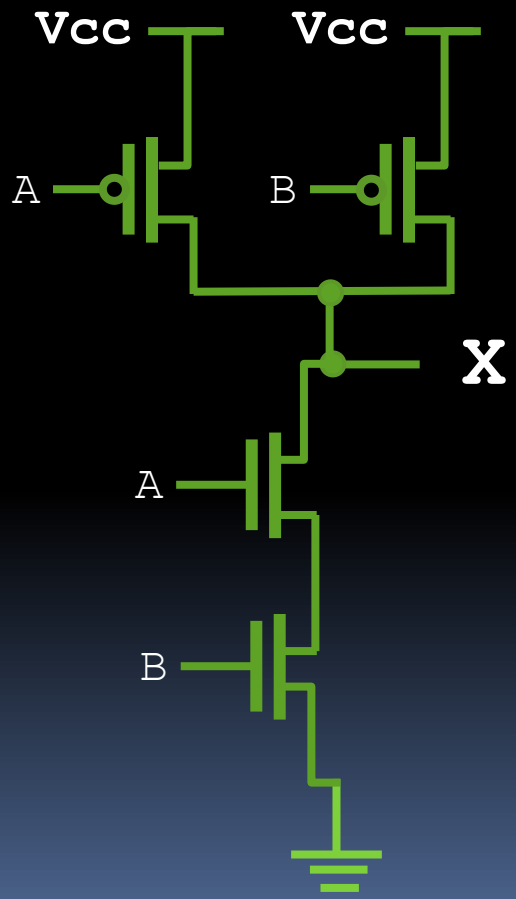
Note that:

- Every input assignment makes a path from output to either Vcc or ground
- Never both.
- Output is never left "floating" (high-Z)
  - There are exceptions



Question 3

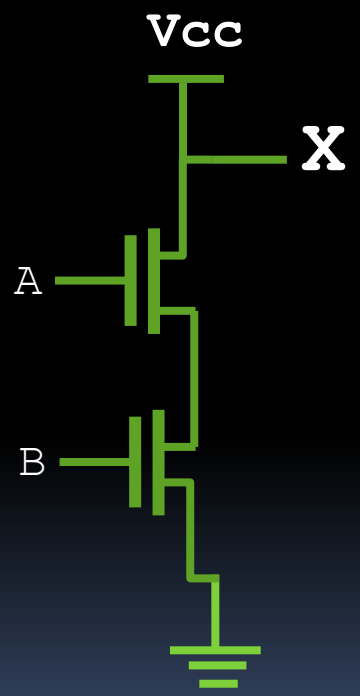
- What gate is created by the following?



Remember: transistors that look like  are activated when the gate input is high, whereas transistors that look like  are activated when the gate input is low.

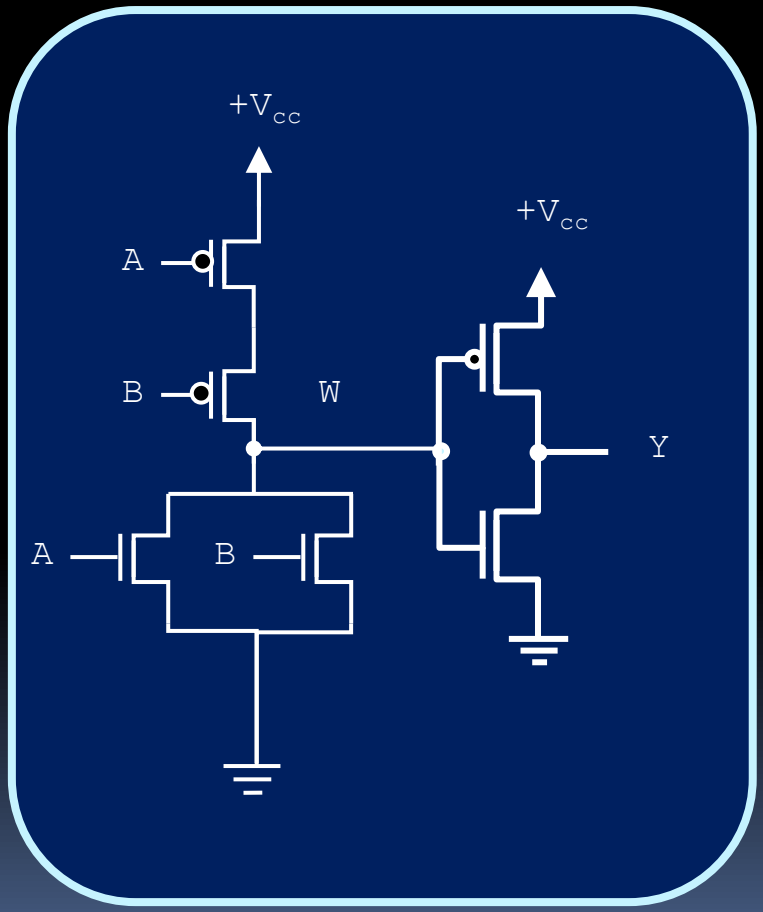
Question 4

- What gate is created by the following?



Note: this is not CMOS

Question 5: Which gate is this?

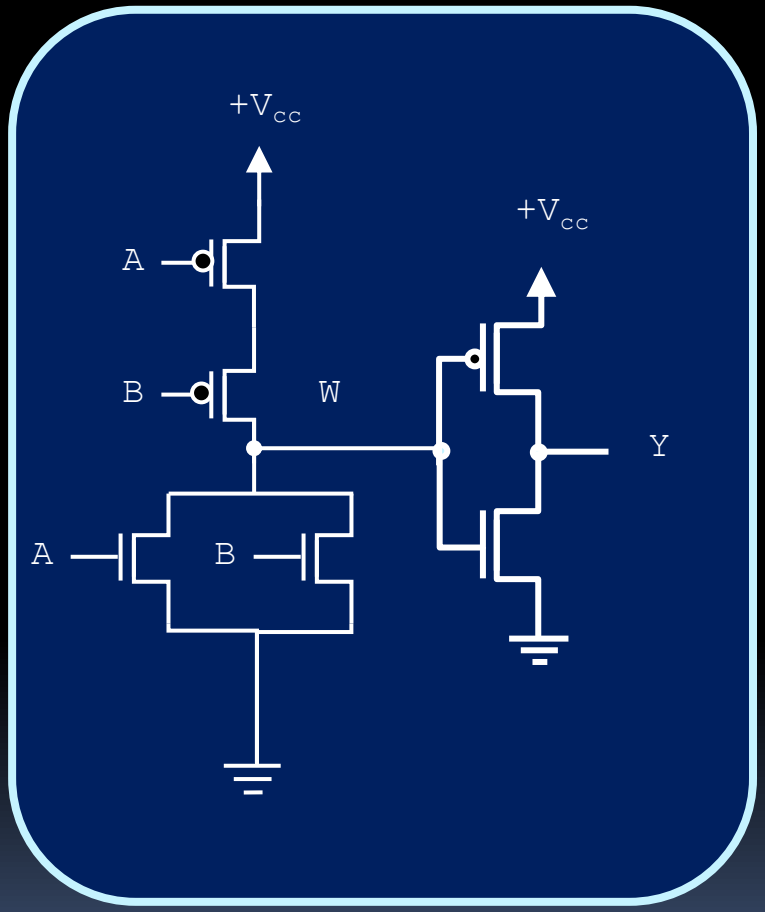


A	B	W	Y
0	0		
0	1		
1	0		
1	1		

W =

Y =

Which gate is this one?



A	B	W	Y
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

$$W = \overline{(A + B)}$$

$$Y = (A + B)$$

Question 6: Bonus Practice