CSC B58 Winter 2018 Midterm Test
Duration — 1 hour and 50 minutes
Aids allowed: none

Student Number: |_|_|_|_|_|_|_|_|_|_|_|_|_|

UTORid: |_|_|_|_|_|_|_|_|_|_|_|_|_|

Last Name: _____ **First Name:** _____

Question 0. [1 MARK]

Read and follow all instructions on this page, and fill in all fields appropriately.

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*Do **not** turn this page until you have received the signal to start.*
(Please fill out the identification section above, **write your name on the back of the test**, and read the instructions below.)
Good Luck!

This exam is double-sided, and consists of 6 questions on 16 pages (including this one). When you receive the signal to start, please make sure that you have all pages.

- If you use any space for rough work, indicate clearly what you want marked.
- Do not remove any pages from the exam booklet.
- Read all instructions before completing any questions
- Write your name and student number on the back of the last page

0: _____/ 1
1: _____/ 4
2: _____/ 4
3: _____/10
4: _____/ 6
5: _____/ 5
6: _____/10

TOTAL: _____/40

Total Pages = 16

[Use the space below for rough work. This page will not be marked unless you clearly indicate the part of your work that you want us to mark.]

Question 1. [4 MARKS]

Draw a circuit (built from transistors) for a XNOR gate.

[Use the space below for rough work. This page will not be marked unless you clearly indicate the part of your work that you want us to mark.]

Question 2. [4 MARKS]

Consider the Verilog code below:

```
module mystery(A, B, Clk, C, D);
    input A, B, Clk;
    output reg C, D;

    always @ (A, B, Clk)
       if (Clk & (A | B))
          begin
          if (A & ~B)
             D = 1;
          else
             D = 0;
          if (B & ~A)
             C = 1;
          else
             C = 0;
          end
 endmodule
```

Briefly explain what this module does:

[Use the space below for rough work. This page will not be marked unless you clearly indicate the part of your work that you want us to mark.]

Question 3. [10 MARKS]

Consider the circuit description given below:

```
If A is high, we want X to have the same value as B, if A is off and C and D are
both high, X should be on. Y acts as A XOR B whenever C is high.
```

Part (a) [2 MARKS]

Draw the truth table

[Use the space below for rough work. This page will not be marked unless you clearly indicate the part of your work that you want us to mark.]

Part (b) [8 MARKS]

Use K-map reduction to produce a SOM expression of X and a POM expression for Y. Show your work.

[Use the space below for rough work. This page will not be marked unless you clearly indicate the part of your work that you want us to mark.]

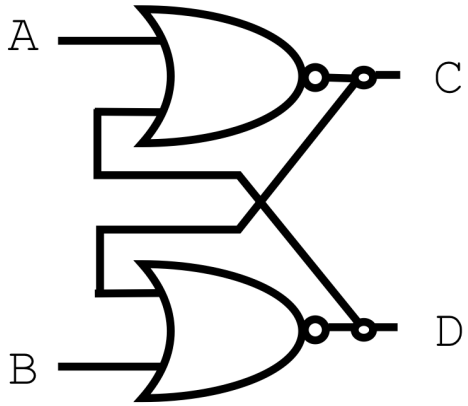
Question 4. [6 MARKS]

Calculate `-13d` * -7d using booth's algorithm. Show your work.

[Use the space below for rough work. This page will not be marked unless you clearly indicate the part of your work that you want us to mark.]

Question 5. [5 MARKS]

Complete the temporal truth table (time going down) for the given circuit



time	A	B	C	D
0	0	0		
1	0	1		
2	0	0		
3	1	0		
4	0	1		

[Use the space below for rough work. This page will not be marked unless you clearly indicate the part of your work that you want us to mark.]

Question 6. [10 MARKS]

Consider the system described below:

> The alarm system can be toggled between armed and disarmed mode by flipping the 'arm/disarm' switch. In armed mode, if the alarm is tripped, it will go into active mode causing a siren to sound. The alarm shouldn't do anything in disarmed mode. When the system is in active mode, it will stay that way until the 'arm/disarm' button is pressed, which will put it back into disarmed mode. Also, there is a debug switch which will put it into maintenance mode no matter what it's currently doing. Once the debug switch is turned off, the system goes into disarmed mode.

Draw the FSM diagram for this system, and give the flip-flop assignment for each state.

Last Name: _____ **First Name:** _____